

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : Not Yet Assigned Confirmation No.:
Applicants : Narain D. Arora, et al.
Filing Date : March 22, 2004
Title : Measurement of Integrated Circuit Interconnect Process Parameters
Group Art Unit : Not Yet Assigned
Examiner : Not Yet Assigned
Docket No. : 700693-4026
Customer No. : 34313

Commissioner for Patents
PO Box 1450
Mail Stop Fee-Amendment
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

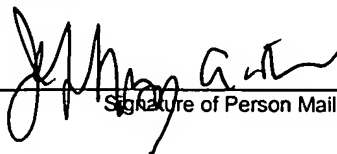
In accordance with 37 CFR §§ 1.97 and 1.98, the items identified in this Information Disclosure Statement ("IDS") are brought to the attention of the Office. The items are listed on the attached form PTO-1449 and copies are enclosed for the convenience of the Examiner.

The items identified in this IDS may or may not be "material" pursuant to 37 CFR § 1.56. The submission thereof by Applicant is not to be construed as an admission that any such patent, publication or other information referred to therein is material or considered to be material (37 CFR § 1.97(h)), or even qualifies as "prior art" under 35 USC § 102 with respect to this invention unless specifically designated by Applicant as such.

CERTIFICATE OF MAILING
37 CFR §1.10

Date: March 22, 2004
Express Mailing Label No.: EV 304439475 US

I, Jeffrey Miller, hereby certify that on the dated listed above, this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service in accordance with 37 C.F.R. § 1.10 as "Express Mail Post Office to Addressee," with sufficient postage in an envelope addressed to: Mail Stop Patent Application, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



Signature of Person Mailing Document

Applicant : Narain D. Arora
Appl. No. : Not Yet Assigned
Examiner : Not Yet Assigned
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INFORMATION DISCLOSURE STATEMENT FILING PROVISION:

☒ This IDS is believed to be timely in that it is being submitted under 37 CFR § 1.97(b), that is (1) within three months of the filing date of the application, which is not a continued prosecution application filed under § 1.53(d); or (2) within three months of entry of the national stage as set forth in 37 CFR § 1.491; or (3) before the mailing of a first Office action on the merits; or (4) before the mailing of a first Office action after filing a request for continued examination under § 1.114. Thus, no fee is required.

☐ However, if the undersigned is in error in this regard, Applicant respectfully requests that the Office consider this IDS as filed under 37 CFR § 1.97(c), if applicable, and charge the fee due under 37 CFR § 1.17(p) to the deposit account referenced below.

☐ However, if the undersigned is in error in this regard, Applicant respectfully requests that the Office consider this IDS as filed under 37 CFR § 1.97(c), if applicable, and a statement under 37 CFR § 1.97(e) is included below, thus no fee is required.

☐ This IDS is being submitted under 37 CFR § 1.97(c), that is after mailing of a first Office action on the merits, but before a Final Action under 37 CFR § 1.113 or a Notice of Allowance under 37 CFR § 1.311.

☐ The fee due under 37 CFR § 1.17(p) is submitted herewith.

☐ A statement under 37 CFR § 1.97(e) is included below, thus no fee is required. In the event that this IDS is not received before a Final Action or a Notice of Allowance, then Applicant respectfully requests that the Office consider the filing of these papers to be submitted under 37 CFR § 1.97(d) and charge the fee due under 37 CFR § 1.17(p) to the deposit account below.

☐ This IDS is being submitted under 37 CFR § 1.97(d), that is after a Final Action under 37 CFR § 1.113 or a Notice of Allowance under 37 CFR § 1.311, but before payment of the issue fee. A statement under 37 CFR § 1.97(e) is included below. The fee due under 37 CFR § 1.17(p) is submitted herewith.

Applicant : Narain D. Arora
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STATEMENT UNDER 37 CFR § 1.97(e):

- ☐ Each item contained in this IDS was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS.
- ☐ No item contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing this statement after making reasonable inquiry, no item of information contained in this IDS was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this IDS.

PAYMENT AND/OR AUTHORIZATION TO CHARGE FEES:

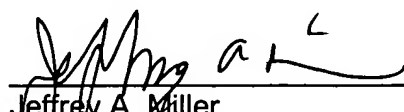
- ☐ A check in the amount of _____ is enclosed for the above fee(s).
- ☐ Please charge \$_____ to Deposit Account No. **15-0665** for the above fee(s).
- ☐ The Commissioner is authorized to charge any fees required by the filing of these papers, and to credit any overpayment to Orrick, Herrington & Sutcliffe's Deposit Account No. **15-0665**.

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: March 22, 2004

By: _____


Jeffrey A. Miller
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FORM PTO-1449 (10-96 MODIFIED)
LIST OF PUBLICATIONS FOR APPLICANT'S
INFORMATION DISCLOSURE STATEMENT

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				<i>Complete if Known</i>		
				Application Number		Not Yet Assigned
				Filing Date		March 22, 2004
				First Named Inventor		Narain D. Arora
				Group Art Unit		Not Yet Assigned
Examiner Name		Not Yet Assigned				
Sheet	1	of	2	Attorney Docket Number	700693-4026	

U.S. PATENT DOCUMENTS							
Examiner Initials*		Document No.	Date	Name of Patentee or Applicant	Class/SubClass	Filing Date (if appropriate)	
	AA	5,999,010	12/07/1999	Narain D. Arora, et. al.	324/765	12/08/1997	
	AB	6,291,254	09/18/2001	Shih-tsun Alexander Chou	438/18	02/04/1999	
	AC	6,312,963	11/06/2001	Shih-Tsun Alexander Chou	438/18	02/04/1999	
FOREIGN DOCUMENTS							
Examiner Initials*		Document No.	Publication Date	Country	Class/SubClass	Translation	
						Yes Abstract	No
						<input type="checkbox"/>	<input type="checkbox"/>
						<input type="checkbox"/>	<input type="checkbox"/>

OTHER DOCUMENTS		
Examiner Initials*		Author, Title, Date, Pertinent Pages, Etc.
	CA	N.D Arora, L. Song, S. Shah, K. Joshi, K. Thumaty, A. Fujimura, J.P. Schoelkopf, H. Brut, M. Smayling, T. Nagata; Cadence Design Systems, San Jose, CA 95135; STMicroelectronics, Crolles, France, 38926; Applied Materials, Santa Clara, CA 95054; Test Chip Characterization Of X Architecture Diagonal Lines For Soc Design; 5 pages.
	CB	Narain D. Arora; Cadence Design Systems, Inc., San Jose, CA 95134, USA; Modeling And Characterization Of Copper Interconnects For Soc Design; 6 pages.
	CC	Dae-Hyung Cho, Man-Ho Seung, Nam-Ho Kim, and Hun-Sup Park; Measurement And Characterization Of Multi-Layered Interconnect Capacitance For Deep Submicron Vlsi Technology; 4 pages; Proc. IEEE 1997 Int. Conference on Microelectronic Test Structures, Vol, 10, March 1997.
	CD	James C. Chen, Dennis Sylvester, and Chenming Hu; An On-Chip, Interconnect Capacitance Characterization Method With Sub-Femto-Farad Resolution; 7 pages; Vol. 11, No. 2, May 1998.

OTHER DOCUMENTS		
Examiner Initials*		Author, Title, Date, Pertinent Pages, Etc.
	CE	Narain D. Arora and Li Song; Atto-Farad Measurement And Modeling Of On-Chip Coupling Capacitance; 1 of 3 pages; IEEE Electron Device Letters, IEEE Transactions on Semiconductor Manufacturing, Vol. 25, No. 2, February 2004.

Examiner Signature		Date Considered	
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- * **EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.